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Enhancement of Cascaded Multilevel Inverter for Solar Power Applications

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***Abstract*- In this paper different modulation methods have been reviewed for the control of Cascaded Multilevel Inverter (CMLI). The main function of CMLI is to synthesize the desired AC output based on the series connection of DC sources (Solar Panels) with reduced power quality issues. Nowadays, it has been recognized as important alternative resource in low/medium voltage solar powered inverter market. CMLI with reduced common mode voltage rejection and reduced number of power switches are also investigated in this paper. To reduce the counts of DC source, a concept of Z-source interfaced CMLI system is introduced. This paper provides a general survey of modulation techniques and further development of CMLI topology.**

Keywords- Multilevel DC link inverter, Z-source network, Space vector modulation.

I. INTRODUCTION

Multilevel converters are classified as diode clamped inverters, flying capacitor inverters and cascaded inverters. DC link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But CMLI is considered as having the simplest structure. CMLI provides a compounding of voltage levels leading to extremely low harmonics. Another advantage is that the bulk inverter may be commercial off the projection, requiring that only the lower power condition inverter to be custom made. So the cascaded inverter has been widely studied and used in fields of Static VAR Compensators (SVCs), power line conditioner and voltage stabilizer. It may be noted that due to other advantages of the modularized circuit layout and package, the cascaded inverter could be a good choice in higher voltage motor drive applications as well as pre-mentioned branches [1]-[2]. The advantages of CMLI get degraded because of more number of power switches and DC sources. To minimize the degradation of CMLI, a new structure of multilevel DC link inverter and impedance source network are developed [3-4]. Various modulation processes were analyzed with a powerful and mathematically rigorous method that provides the analytical expressions of the output phase voltages of the inverter. This paper is organized as follows; Section I shows the classification of power converters. Analyses of different switching patterns are addressed in Section II. Section III shows the general introduction of multilevel DC link inverter. Analysis of Multilevel Inverter (MLI) with Z-source network system is reviewed in Section IV and Section V concludes the survey for the further development of CMLI.

Fig.1 illustrates the classification of converter families used in lower power and high power drive applications, which have a basic division into direct and DC link topologies. Cyclo-converter and matrix converter are the direct conversion topology used in lower power and high-power applications respectively. This conversion uses an array of power-semiconductor switches to connect directly the power supply to the machine, converting a three phase AC voltage with a fixed magnitude and frequency to a three phase AC voltage with variable magnitude and variable frequency. On the other hand, indirect converters are classified into current-source and voltage-source topologies, depending on the dc-link energy storage component. For high power applications, two Current Source Inverter (CSI) topologies have found industrial presence: the Load Commutated Inverter (LCI) and the PWM based CSI. The LCI has been used for several decades featuring simple converter topology, low manufacturing cost, and reliable operation. Voltage Source Inverter (VSI) has found more attention towards industrial and commercial applications. The classifications of VSI are 2-level VSI and MLI systems.

The darkened boxes in the classification are the focused systems in the paper. The MLI systems have experienced a higher market penetration and a more noticeable development over the last decade, in comparison to other topologies. Among MLI topologies, CMLI provides tremendous advantageous towards solar powered applications. The general structure of CMLI for single phase and three phase system is shown in Fig. 2.

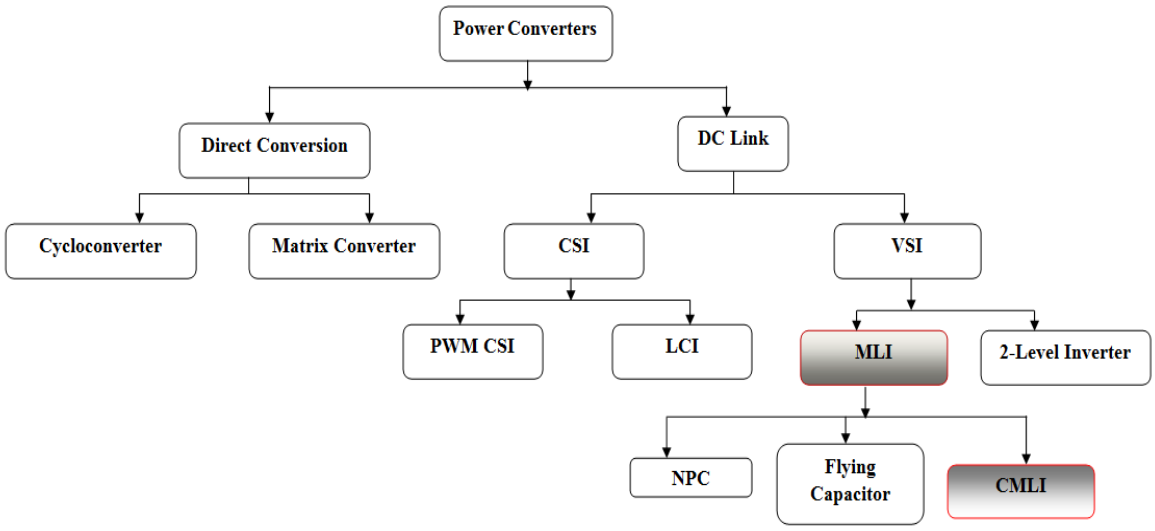

Fig. 1. Classification of power converters

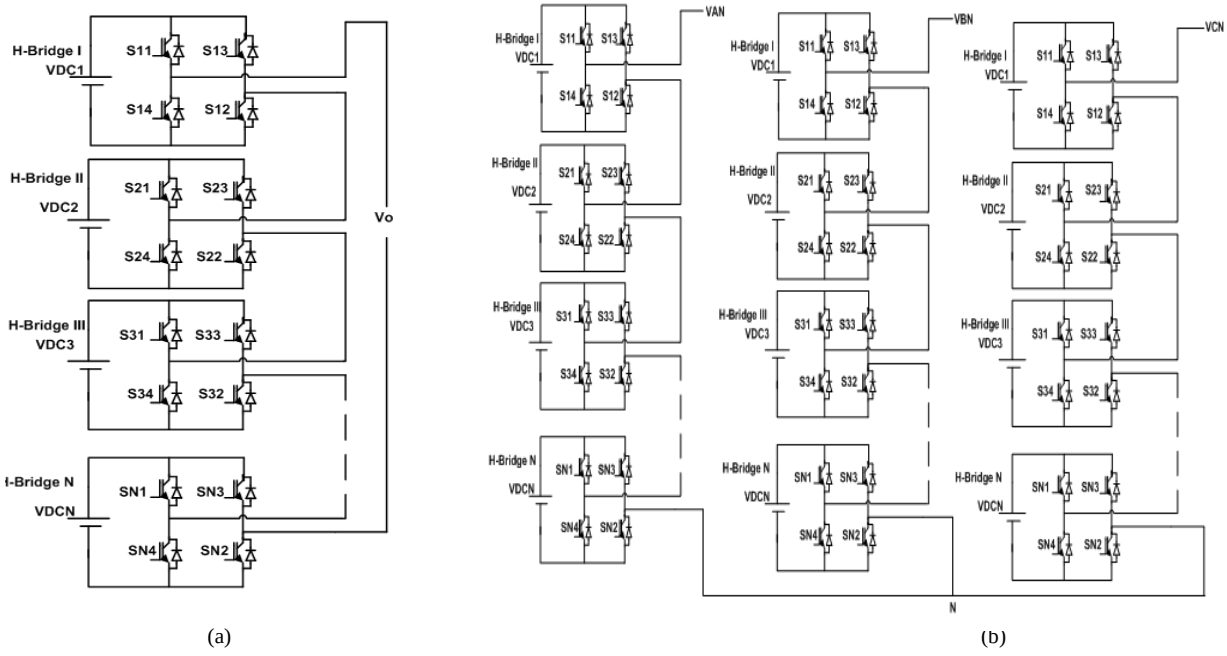

Fig. 2. Cascaded multilevel inverter (a) Single phase system (b) Three phase system

Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore Electromagnetic Compatibility (EMC) problems can be reduced. It draws input current with low distortion. Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It has lower switching loss and higher efficiency. In the cascaded H-bridge multilevel inverter each level requires a separate DC source and for each DC source a PV cell is to be connected. In CMLI, each solar module is isolated from load side.

II. Analysis Of Modulation Techniques

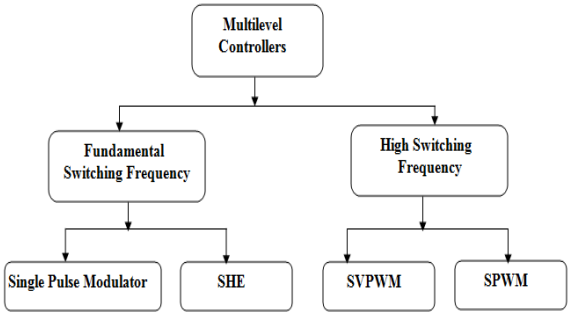

Fig. 3. Classification of multilevel controllers

The general classifications of multilevel controllers are shown in Fig. 3. Commonly used stair case modulation scheme produce common mode voltages. Common mode voltages may affect the motor shaft voltages and bearing currents. There has been a number of mitigation techniques suggested for the bearing current problem and conducted Electro Magnetic Interference (EMI) [5]. Space Vector Pulse Width Modulation (SVPWM) and Sine Triangle Pulse Width Modulation (STPWM) schemes are suggested for the control of CMLI to eliminate common mode voltages and to obtain better power quality. The various modulation techniques are as follows:

A. Staircase pulse switching pattern

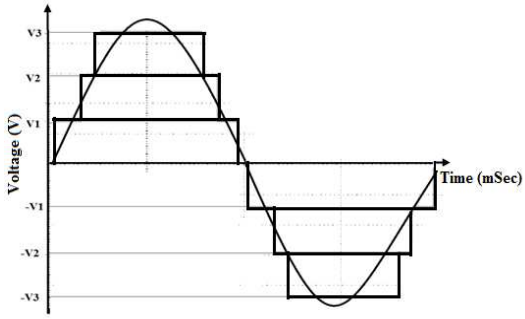

Fig. 4. Staircase switching pattern

Staircase switching pattern of seven-level CMLI is shown in Fig.4. The switching states of CMLI switches are: $V_0 = 0V$, when all switches are in OFF state, $V_0 = (V_{dc}/3)$, when S_1 & S_2 switches are in ON state, $V_0 = (2V_{dc}/3)$, when S_1, S_2, S_5 & S_6 switches are in ON state, $V_0 = V_{dc}$, when S_1, S_2, S_5, S_6, S_9 & S_{10} switches are in ON state. $V_0 = (-V_{dc}/3)$, when S_3 & S_4 switches are in ON state, $V_0 = (-2V_{dc}/3)$, when S_3, S_4, S_7 & S_8 switches are in ON state, $V_0 = (-V_{dc})$, when S_3, S_4, S_7, S_8, S_{11} & S_{12} switches are in ON state [6].

B. PWM technique based switching pattern

Improved output voltage can be obtained through PWM switching of multilevel inverter switches. The improvements in the harmonic contents due to the increased number of levels (N) were highlighted. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy. Other authors have extended two level carrier based PWM techniques to multilevel inverters by making use of several triangular carrier signals and one reference signal per phase. Third harmonic injection based PWM and multicarrier PWM switching techniques were developed to reduce the harmonic content in the system output. For N-level inverter, carriers with the same frequency and same peak to peak amplitude are disposed. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched ON, and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched OFF.

Third harmonic injection based PWM pulse is shown in Fig.5 (a). Fig.5 (b) shows the developed AC output voltage of CMLI under third harmonic injection based PWM pulses. Multicarrier PWM (MCPWM) is one the most common switching strategy for CMLI with an improved harmonic performance [7-11]. Each single phase inverter is controlled using three-level modulation which leads to cancellation of all carrier and associated sideband harmonics. MCPWM pulse generation and developed AC output voltage is shown in Fig. 6 (a & b).

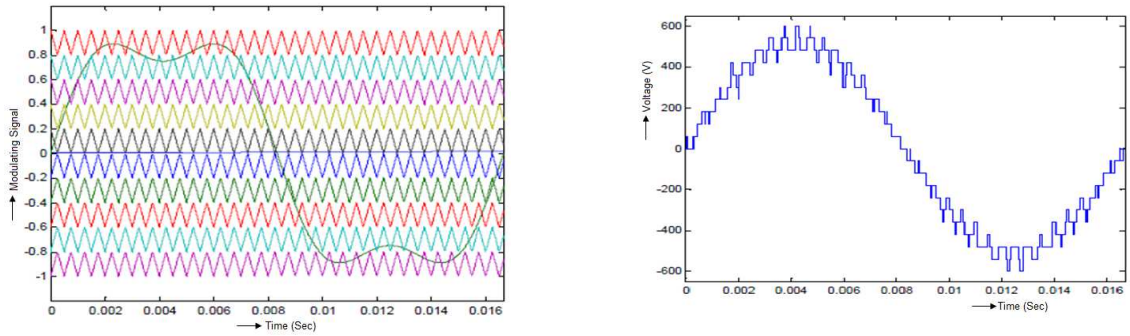

Fig. 5. Third harmonic injection (a) PWM pulse generation pattern (b) Output Voltage

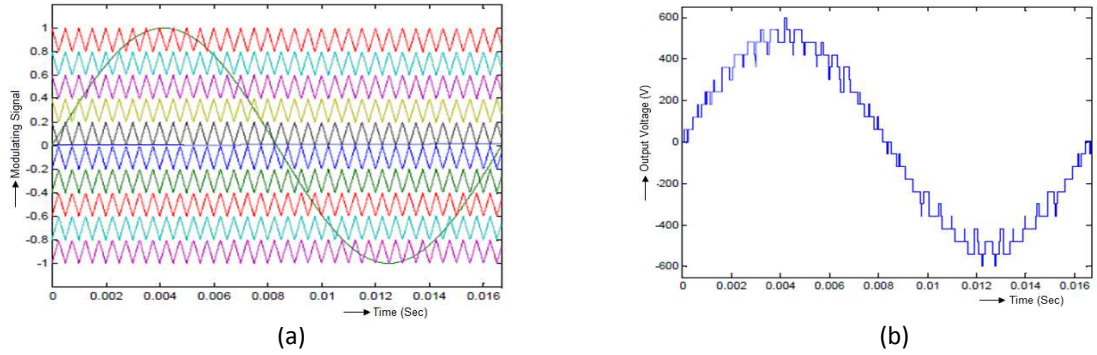

Fig. 6. Multicarrier (a) PWM pulse generation pattern (b) Output Voltage

C. *Joint Inverter Control*

The method of joint inverter control is proposed to utilize nine-level modulation followed by a Redundant State Selection (RSS) table for voltage balancing [12]. The pulse generation pattern and the generated reference pulses of joint inverter control are shown in Fig. 7.

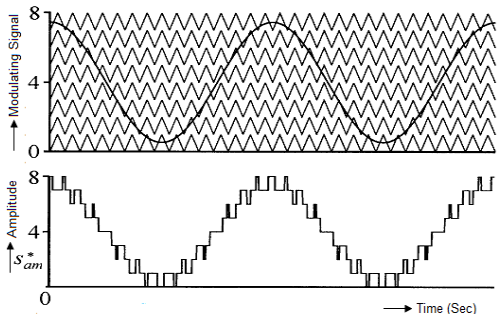

Fig. 7. Joint inverter control switching pattern

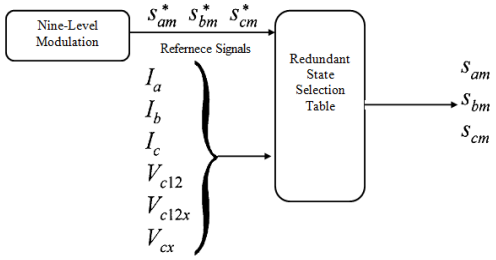

Fig. 8. Joint inverter control rredundant state selection

The modulation is typically programmed in a Digital Signal Processor (DSP) and may be followed by an RSS table located in either the DSP or in a Programmable Logic Device (PLD). The inputs and outputs of RSS selection table is shown in Fig. 8.

Generally, SPWM schemes are more flexible and simpler to implement, but the maximum peak of the fundamental component in the output voltage is limited to 50% of the DC link voltage, and the extension of the SPWM schemes into over modulation range is difficult.

D. Multilevel SVPWM

In SVPWM schemes, a reference space vector is sampled at regular intervals for determination of the inverter switching vectors and their time durations, in a sampling interval. The SVPWM scheme gives more fundamental voltage and better harmonic performance compared to the SPWM schemes [13]-[20]. The maximum peak of fundamental component in output voltage obtained with space vector modulation is 15% greater as compared with sine-triangle modulation scheme. Multilevel converters have a large number of vector states which can be used to modulate the reference signals (sinusoidal signals). Each state vector has a number of redundancies. Multilevel SVPWM provides modulating vectors with an appropriate switching sequence. However, the same properties of state and switching redundancy allow the improvement of the modulation technique to fulfill additional objectives like reducing the common mode output voltage, reducing the effect of over modulation on the output currents, improving the voltage spectrum. In SVM scheme inverter switching states are shown in Fig. 9.

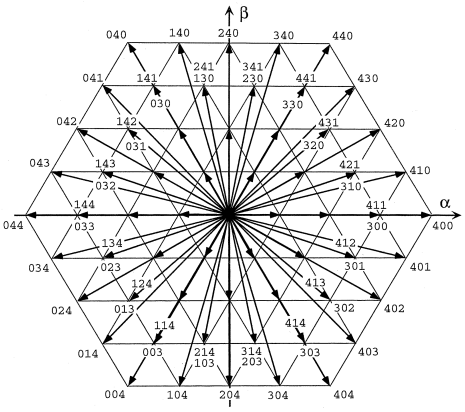

Fig. 9. SVPWM based switching states

III. MULTILEVEL DC LINK INVERTER

General structure of CMLI shown in Fig.2 has more number of power switches. To reduce the power switches in the conventional CMLI the proposed multilevel DC link inverter is reviewed, which consists of number of DC source connected in series through power switching devices and a Single Phase Full Bridge (SPFB) inverter [3]. The general structure of multilevel DC link inverter is shown in Fig. 10. The level of output voltage is decided by the proper switching of DC link switches. The number of power switches gets minimized through the proposed multilevel DC link inverter.

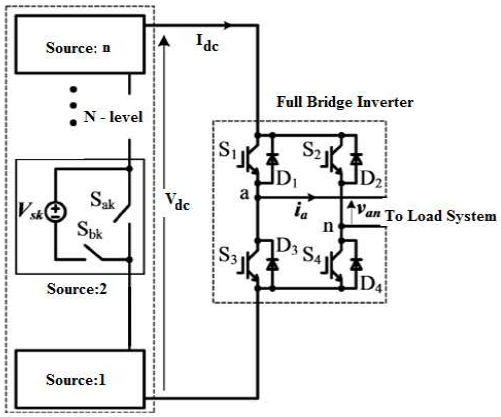

Fig. 10. Multilevel DC link inverter

The number of power switches gets minimized through the proposed multilevel DC link inverter. Two switches S_{ak} and S_{bk} operate in a toggle fashion. Each DC source is connected through the toggle fashion operation of S_{ak} and S_{bk}. Through full bridge inverter, the DC link voltage (Vdc) is converted into AC voltage.

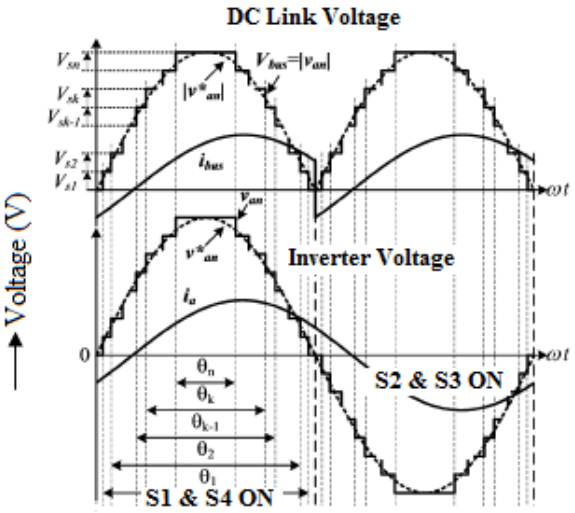

Fig. 11. Output waveforms of DC link inverter

The output voltage of multilevel DC link inverter is shown in the Fig. 11. The voltage across the DC link is equivalent to that of the full wave rectifier. Through the proper switching of single phase full bridge inverter switches the DC link voltage is converted to AC voltage. The output voltage waveform of multilevel DC link inverter is develpoed through staircase pulse switching pattern.

Number of switches required for conventional CMLI is N = 2*(m-1)
Number of switches required for DC link MLI is N = (m+1)

IV. MLI WITH Z- SOURCE NETWORK

To reduce the DC source counts, boost or buck operation of MLI output voltage is required. To achieve both boost and buck operation, Z-source based CMLI is recommended through this review paper. The equivalent circuit of cascaded Z-Source CMLI is shown in Fig. 12. It consists of single phase H-bridge inverter units, Z-source network and DC sources (I, II, III) [4] & [21]. Each H-bridge Z-source CMLI can generate three different stages output voltage $+V_{in}$, 0, $-V_{in}$. Output voltage can be higher than the input voltage when boost factor, B > 1. Boost operation can be achieved by shoot through state of switching and buck operation is achieved by non-shoot through state of switching of inverter switches.

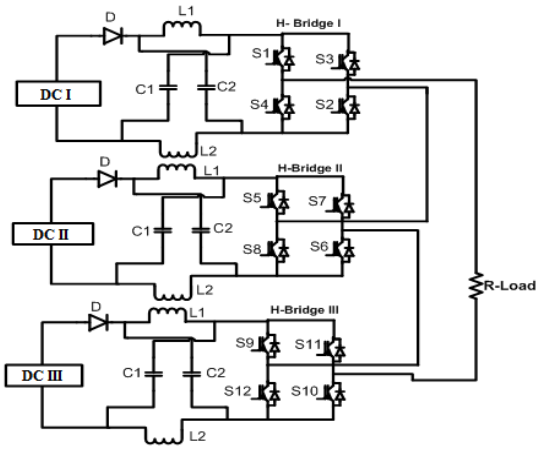

Fig. 12. Equivalent Circuit of Z-Source MLI

V. CONCLUSION

This paper presents the idea about the possible modulation technique for cascaded multilevel inverter. The proposed paper also reviewed the multilevel DC link inverter topology and its unique advantages. Buck and boost operation of multilevel inverter output voltage is achieved through the impedance source network.

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