

Multiple Task Migration in Mesh Network on Chips over virtual Point-to-Point connections

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Abstract

Multiple task migration in a network on chips is able to transfer the data from one cluster to another cluster, while transfer the data from one cluster to another cluster message latency, migration latency, Network latency and power consumption are problem encountered. New techniques are introduced like hybrid scheme, virtual point to point Connections (VIPs) has been introduced that dedicates low power and low latency heavy communication flow created by multiple task migration mechanism. The proposed system scheme reduces total message latency, total migration latency, total network latency, power saving is achieved compared to the previously proposed task migration strategy for mesh multicomputer. Analyzing the results show that the proposed scheme reduces message latency by 16% and migration latency by 15%, while 13% power savings can be achieved.

Keywords: MPSoCs, NoCs, Task migration, Virtual point-to multipoint connection, Performance, Power.

1. Introduction

In earlier days point to point links, star based approach and shared buses which increases large number of IP cores on the same chip makes the design of communication architectures involves major problems in SoCs. In this earlier approach increases vast area and also poor scalability are the major drawbacks while connecting point to point communication links in SoCs, Applicability of shared buses and star based communication to future many core SoCs are also under question due to unpredictability of latency and enhancement of power. [3, 10]. To reduce the area and increases the efficiency of packet switched network on chips are precisely performed and computes in present generations of multiprocessor systems on chips. Experimental results of various on-chip interconnection design shows in [10] where the authors compare various on-chip interconnections and NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs. NoC applies networking theory and methods to on-chip intercommunication and brings notable improvements over conventional bus and crossbar interconnections.

Network on chip is an emerging paradigm for communications with in large VLSI systems implemented on single silicon chip. In NOC systems, modules such as processor cores, memories and specialized IP blocks exchange data using a network as a “public transportation” sub-systems for the information traffic. A NOC establishes from multiple

point to point data links interconnected by switches, such that messages can releases from any source module to destination module over several links, by making routing decisions at switches. Generally heterogeneous MPSOC'S [7] are under progress in applications of multimedia and networking such sorts of operation mechanism created by the dynamic work load, and this technique performs various numbers of tasks running simultaneously in multi processor systems on chip.

In fact heterogeneous MPSOC'S design faces major challenges like communication and computation latency for achieving better reliability and while introduce a deadlock free routing algorithm in generic NOC's architecture [19,12] which minimized communication energy, simultaneously communication system should assists to satisfy the specific design constrains via bandwidth reservation. In a single silicon die consists of number of resources [18] that have to communicate makes the use of interconnection systems based on shared buses are not convenient, a simple technique is used to resolve the problem of on-chip communication is to use a Network on chip communication. This is the best way to resolves that problem of on chip interconnections.

Generally NOC based MPSOC's [7] with dynamic work load which minimize the occupations of NOC's links and also which investigates the reliability of various mapping algorithms. An application of dynamic [22] work load shows even optimal mapping that may not meet best performance; it requires some optimization technique such as task migration.

Task migration in mesh NOC's manipulate free from the congestion and load balancing as major objective. In silicon chip establish network [8, 4, 13, and 16] resources using interconnection while communicating between the nodes/link some may get defects and failures, majorly monitoring constraints as well as space and power limitations, so to resolve such sort of network problems which requires some technique called Hardware/Software portioning algorithm.

On-chip communication supports hundreds of cores in single silicon wafer. Source routing has one major drawback of over head for storing the path information in header of every packet. If the size of the network increases the performance will reduces.[23] Junction based routing can resolves such kind of problems and it has two important issues related to junction based routing, such as numbers and position of the junctions and path computation for efficient dead lock free

Figure 2 show Junction Configurations for Other Kinds of Routing Algorithms such as West-First, XY and Negative-first routing algorithms are applied.

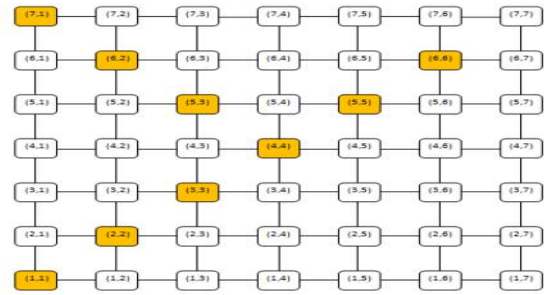


Fig 2. West-First Routing Algorithms

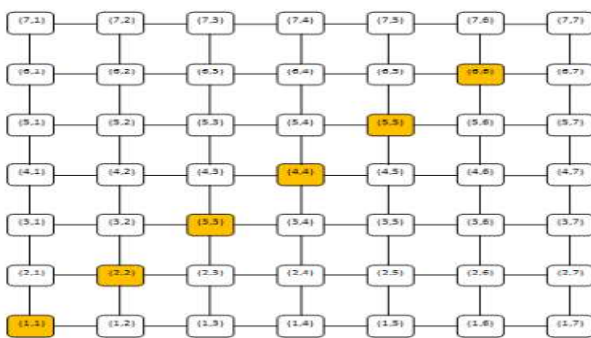


Fig 4. Negative-First Routing Algorithm

routing, while increasing the path length reduces the number of junctions.

The illustration of different routing algorithms about path computations for Mesh topology NOC with junctions figure: 1 shows that junction configurations for North-Last Routing Algorithm. Applying North-last routing algorithm, minimum number of junctions is 9. we define junction ratio as follows:

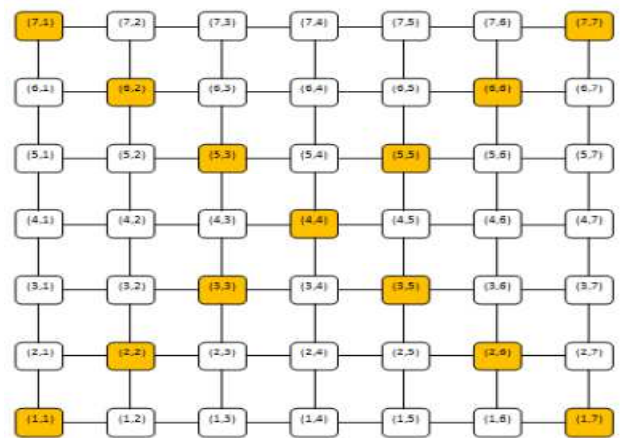


Fig 3. XY Routing Algorithms

For instance, applying XY routing algorithm, number of required junctions is 12. Figure-2, 3, 4 shows the only possible configurations for these routing algorithms used.

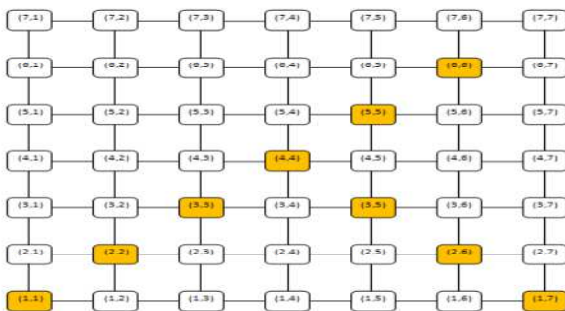


Fig 1. 7x7 Task migration network using North-Last routing algorithm with hop count Limit of 7

$$NJ/NN = \text{Number of junctions/number of Nodes} = 9/49 = 0.18.$$

Figure 1 shows the only possible configuration for this case, the number of available paths are generally reduced when using JBR.

2. Objectives

Runtime task migration [14] was first proposed in multicomputer with load balancing as the major objective. However, specific NoC properties such as limited amount of communication buffers, more sensitivity to implementation complexity, and tight latency and power consumption constraints bring new challenges in using task migration mechanisms in NoCs. As consequence, the efficiency and applicability of traditional migration mechanisms (developed for multicomputers) are under question. Due to the limited resource budget in NoC-based MPSoCs as well as tight performance constraints of running applications, in this paper, we propose an efficient methodology based on virtual point-to-point (VIPS for short) connections. These dedicated VIPs connections provide low-latency and low-power paths for heavy communication flows created by multiple task migration mechanisms.

3. Related work

In earlier days various techniques has been introduced in mesh multi computers such as task migration and multiple task migration [8, 19, 22and 18].In this research paper [8] three types of migration was introduced, such as first migration called as Diagonal scheme major objective is to explore all disjoint paths in one phase to migrate task based on XY routing, second migration called Gather-routing-scattering algorithm express about to optimize the number of task migration paths finite number of nodes in the source sub mesh and send them to the corresponding cores in the destination sub mesh which will then scatter the tasks to their final destinations. The above two migration schemes are combined called hybrid scheme.

In [19], two task migration schemes are introduced in 2D wormhole-routed mesh multicomputer with all ports of communication model. So some constraints are applied for the selection of source and destination sub meshes. Two migration schemes, namely general task migration scheme (G-TMS) and near optimal task migration (NO-TMS).

In paper [22], two migration schemes are discussed namely ODC-SC and ODCFC. Here in this express about to rearrange the active task in the mesh such that larger contiguous area of free nodes will be available for future allocations. The above methods are trying to locating on destination sub mesh similarly when task migrates towards that sub mesh, it creates the minimum interfere with other tasks migrating in the network. The word task migration was recently addressed, the main theme concentrate on the mechanism of starting mechanism on the source core and resuming the task on the destination core.

In paper [14], heterogeneous MPSOC's major challenges are both communication and computation resources while during runtime task management. In the run time task migration is addressed in NOC's based on code checking pointing. The first platform resource is to require fast and efficiency on NOC'S and second thing on NOC's resources reallocation taken place in case of mapping failure and changes by the user requirement. In this approach may concerns only performance while neglecting power consumption.

In paper [4], multi processor systems on chips which showing the interest in migration technique and also arises both in research and product development. The main thing of this paper deals about process migration only and don't consider performance and power consumption over heads of migrations. However it is well suited for single chip multi processors and bus based MPSOC's with distributed operating systems. Here in this paper deals which migration based on code check pointing and user level middleware supports for many MPSOC's application domains.

In paper [6] which deals process of migrate whole code and data transferred from one node to the chosen destination node. This paper mainly concerns evaluate task migration in NOC-based MPSOC's to optimize entire system energy dissipation and to achieve deadlines.

In paper [16, 23] which deals to recognize the defective node occurs in the network links. Here mainly concerns how to reconfigurable defective node/link can be handled, however in this literature survey investigates neither specific task migration nor supporting architecture has been discussed. In the literature survey [2, 4, 5, 6, 7, 13, 14, 23 and 15] says that task migration obviously initialized at the source node which causes stalled execution of the tasks running at the source core, and after that transmission of the task to the destination core, resuming its execution in the destination core. We are mainly concentrating to minimize the power consumption and improve overall network performance while overhead caused by migrating tasks when they are transferring from source core to destination core. Point-to-point paths are used to reduce the task migration time and power overhead also manipulate over normal data flows to service migration process quickly.

4. Problem Formulation

In general 2D Mesh multi computer consists of local memory, processor and router and some input and output function. The architecture of the 2D meshes multicomputer system which provides wormhole routing in all-port communication. In general system level design of 2D mesh multicomputer depends up on graph-based design architecture. In Mesh NOC's interconnects can be represented as some parameters like size, router, bandwidth and buffer.

Size consists of (X and Y) dimension parameters

Router consists of (source, destination)

Bandwidth (BW)

Buffer (B)

The above parameters are essentially preferred in this NOC's architecture.

Now we are dealing with task migration between two sub meshes SM [(x1, y1), (x2, y2)] or SM (W, H) where (x1, y1) and (x2, y2) are respectively, the coordinates are bottom- left and top-right corners of the source sub meshes and SM'[(x3, y3), (x4, y4)] or SM'(W, H) where (x3, y3) and (x4, y4) are respectively, the coordinates are bottom-left and top-right corners of the destination sub meshes in 2D mesh NOC's. It is defined as any IP core of SM to the corresponding IP cores of SM' while other IP cores execute their tasks with no stalled communications. The main objective is to reduce the overhead of migration to the normal communication of other IP cores.

In a network on chip while doing migration from one core to another; it incorporates migration time and power consumption, simultaneously increases the ultimate network

latency. Average migration latency also involved in task migration is defined as average time interval between the source of migration and to reach the last migration flits in the destination sub mesh.

In this research would like to introduce a packet switched network on chips which can also provide low-power and low-latency dedicated virtual point-to-point (VIP) paths between any two nodes by bypassing the pipeline of the intermediate routers.[12,22] A virtual channel of physical is designated to bypass the router pipeline stages. In this paper buffer is replaced by a register (1-flit buffer) which holds the flits arriving on the virtual channels.

Figure 5. show the architecture of router implementation details of one input port and one output port and also VIP is connected between any two given nodes. The router uses a multiplexer-tree-based crossbar fabric, since a packet a packet coming through an input port does not loop back, each multiplexer is connected to three input ports as well as the local PE. VIP register has to set 1 refers as full i.e., when the register has incoming flits to service. So that signal used to select the multiplexer connecting one of the VCs to the crossbar input. If the register is empty refers as full= 0, usually virtual channel is selected based on the out coming of the routing function. Virtual channel allocation and switch allocation units are traditional role in packet switched networks.

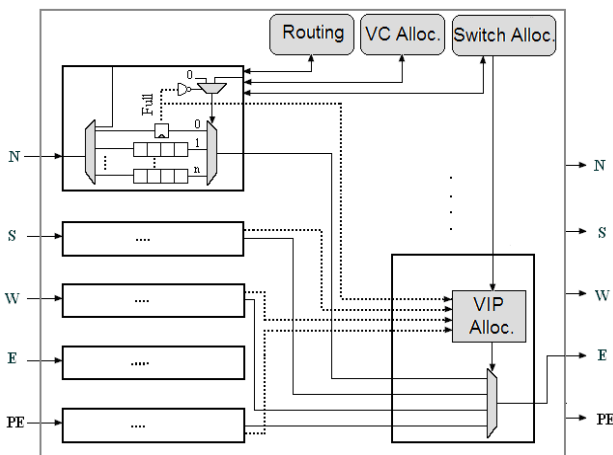


Fig 5. Router Architecture

Otherwise VIP register is directed to the crossbar input. The full signal is used to control the crossbar operation and also it is used to control the arbiter and allocates the output port to the input port of the VIP in the buffer. It seems to be just like traditional role of packet switched network on chips. In some aspects of baseline packet switched router VIPs are involves to adding 1-flit buffer at each input port and VIP allocator at the output port and some 1-flit wires to propagate a signal which has minimal impact on the base line router architecture and imposes a negligible area overhead. Here

VIPs sends corresponding packets using VC 0 of the output port via flits should be transferred.

VIPs are usually allows the packet depends up on order of importance (prioritized) over packet switched network to mitigate the effect of any congestion between normal data packets and VIP data packets. VIPs are allowed huge communication flow via dedicated pipeline link from source core to the destination core. VIP connection should not allow sharing the same link that is each router port can be used by at most one VIP connection. VIP flits are bypass over router pipeline stages and power consumption and delay related to buffer read, write, switch allocator and VC allocators are removed. So the resulting of high communication flow in VIPs takes an advantage of power saving and reduction in average message latency.

5. Proposed approach

The proposed low-power and low-latency task migration strategy is based on hybrid scheme algorithm [8] and uses VIPs [12] for the paths involved in task migration to reduce the average migration latency (AML) and hence the total mean network latency and power consumption.

Hybrid scheme is a combination of both diagonal scheme and gathering-routing-scattering algorithm based on X-Y wormhole routing, and then source sub mesh makes in to several rectangular sub partitions which consists of size i.e. $p \times q$ as shown in figure 6. Sub partition of mesh SM ($W/p, H/q$) where $W/p, H/q$ are the width and height of partitioned sub mesh. In order to reduce the number of task migration paths, a set of IP cores at the source sub mesh into set of sub partitions are selected to gathering the tasks of the IP cores, located on destination diagonal line, on each row or column in each sub partition, depending on the size of p and q . This approach is similar to Gathering- routing-scattering algorithm and then diagonal scheme should allocate schedules max ($W/p, H/q$) phases is used to route the accepted subtasks to their corresponding core. In the first step, each sub partition is represented as sub core is used to distribute its subtasks on each core to their corresponding destination core. Hence scattering scheme is used to transfer subtasks on each row or column in each super core to complete the multiple task migration.

In this approach we are mainly concentrating on power consumption, network latency, message latency and migration latency. The process of multiple task migration is used to transfer the data from one core to another core, so it utilizes some mechanism that is hybrid scheme. In the hybrid scheme the first process is used to collect each sub task in each sub core and each row or column; hence it is congestion free. In addition to that there is congestion when node is located on the diagonal scheme in each sub core migrates its combined sub tasks to its corresponding core. The next process is used combined the previous steps such as Gathering and diagonal

scheme. Finally the last process is used to take place that is scattering scheme which is response to transfer each sub task to their nodes of each row or column in each sub core. Using this technique number multiple task migration flows are reduced. Hence Hybrid scheme is congestion free for each phase.

Gathering step obtaining derivation of time calculated as

$$T_{gather} = \max([\log_e p], [H/q]) * t_s + \max([\log_2 p^{m^2}], [\log_2 q^{m^2}]) * t_x$$

t_s = startup latency
 t_x = link between the neighboring nodes
 m = number of flits.

Diagonal step obtaining derivation of time calculated as

$$T_{diagonal} = \max([W/p], [H/q]) * (t_s + \max(m p, m q) * t_x)$$

Finally scattering scheme obtaining derivation of time calculated as
 $T_{scatter} = T_{gather}$ here it obtains the time taken by the scatter is square of that time taken by the gathering process.

Total transmission time (hybrid time) is combined of all above parameters such gathering time, diagonal time and scatter time.

There fore $T_{hybrid} = T_{gather} + T_{diagonal} + T_{scatter}$

The process of hybrid scheme is involved in multiple task migration as shown in figure below

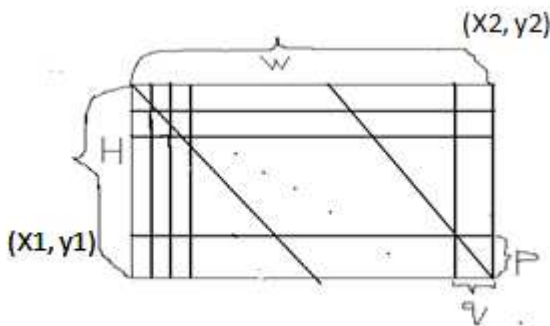


Fig. 6. Sub meshes incase $w > h$

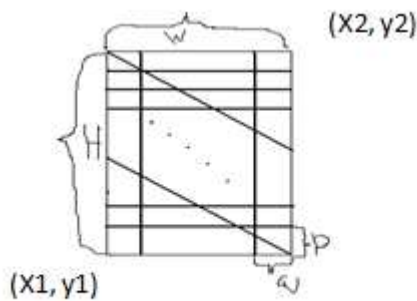


Fig. 7 Sub meshes incase $w < h$

VIPs are connected in the form of peer-peer from source sub mesh to destination sub mesh. The performance of packet switched NOC's architecture uses light weight [12, 22] setup network to control VIPs establishment. Suppose if there are no sufficient resources from new VIP connection request that new VIP can tear down old VIPs. The strange new VIP is provides a weight based on the channel required. In the proposed multiple task migration strategy, VIPs is prioritizing formed for multiple task migration over other possible VIPs built for normal high volume communication flows.

6. Experimental Results

In this section, we evaluate the proposed Mutiple task migration schemes using *Gathering-Routing-Scattering* algorithm [8]. All considered mutiple task migration strategies and the proposed technique are implemented on an NoC architecture simulated by Xmulator [2]. Xmulator [2] is a fully-parameterized discrete event simulator for interconnection networks which is augmented with Orion library [19] to calculate the power consumption of the network. Also, the hardware and software requirements for VPMPs establishment and control networks are emulated in this environment. Simulation experiments are performed for a 128-bit wide system. Moreover, the process feature size and working frequency of the NoC is set to 65nm and 280 MHz.

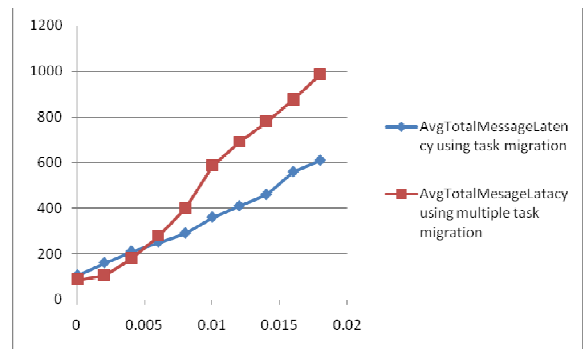


Fig. 5 Average message latency

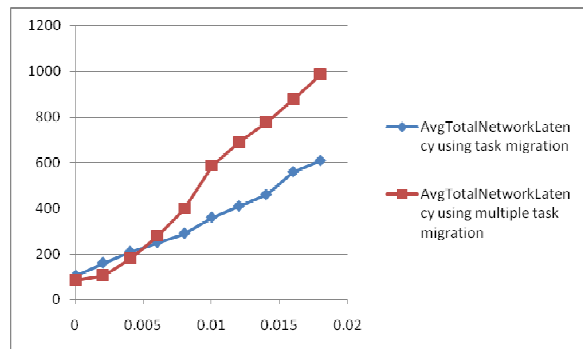


Fig. 6 Average total network latency

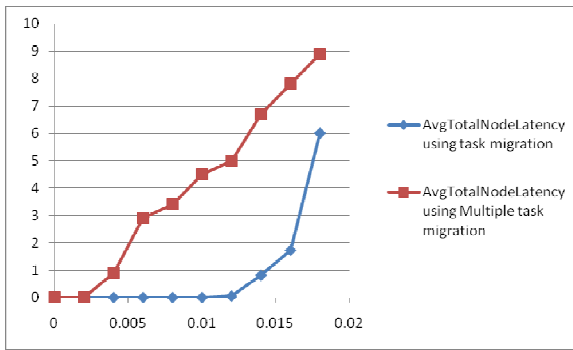


Fig. 7 Average total node latency

In summary, the proposed VPMPs based scheme has reduced the average message latency by 16%, average node latency by 15%, and total network power by 13% with respect to *Gathering-Routing-Scattering* method.

7. Conclusion

In this paper, we proposed multiple task migration schemes in mesh-based NoCs based on low-latency and low-power virtual point-to-point (VIPs) connections. Experimental results revealed that the proposed scheme could improve over earlier technology. This improvement was due to a series of strategies used in the proposed method i.e. multiple task migration was enhanced the message length rate with in short span of latency during VIPs establishment and also pipelining migration VIPs were prioritized over normal VIPs. Since a new VIPs connection could tear down previously established VIPs (if suitable), we could even prioritize scenarios with multiple task migration and hence network performance improvement can be achieved. In future we can expect some more enhancement using virtual point-to-multi point connection in the presence of super scalar methodology which will provides low latency and low power heavy communication flow created by multiple task migration mechanism.

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